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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/706,212	11/12/2003	Michael E. Connell	5083.1US (01-0428.01/US)	6326

24247 7590 03/06/2006

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EXAMINER	
WILSON, ALLAN R	

ART UNIT	PAPER NUMBER
2815	

DATE MAILED: 03/06/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

H:A

Office Action Summary	Application No.	Applicant(s)	
	10/706,212	CONNELL ET AL.	
	Examiner	Art Unit	
	Allan R. Wilson	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 January 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2,4-8,10-14,16-20 and 22-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,4-8,10-14,16-20 and 22-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *0505, 0805, 1005, 0106*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1, 2, 4-8, 10-14, 16-20 and 22-24 are rejected under 35 U.S.C. 102(e) as being anticipated by 2003/0017652 to Sakaki et al. Regarding claims 1, 7, 13 and 19, Sakaki teaches in figure3 a semiconductor die comprising:

a semiconductor substrate 1 having a front side 1B and a back side 1A and having a low ratio of height to horizontal dimension (see fig. 2);

an integrated circuit on a portion of the front side (note that the front side is also labeled 1X which is designated the "circuit formation surface");

a passivation layer 7 (resin, para. 0096) covering a portion of the integrated circuit causing a stress on at least a portion of the substrate; and

a stress or force balancing layer 2 covering at least a portion of the backside substantially balancing the stress caused by the passivation layer covering a portion of the integrated circuit (see paras. 0106 and 0107, esp. 0107 at the third sentence *et. seq.*, which teach that layer 7 causes a stress which is compensated by layer 2), the stress or force balancing layer comprising at least

one of a tape material (2 in FIG. 8) for balancing stresses in more than one direction[1] and an adhesive material (paragraph 127, layer 2 is thermally adhered to substrate 1). Additionally, "a chemical vapor deposition material" and "a physical vapor deposition material" are product by process limitations (see MPEP 2113).

Regarding claims 2, 4, 8, 10, 14, 16, 20 and 22, Sakaki teaches that the balancing layer is a resin, which may be considered either a single component layer or a homogenous mixture of a strong material, is an adhesive (as it adheres to substrate 1) and may be marked by a laser (an intended use).

Regarding claims 5, 6, 11, 12, 17, 18, 23 and 24, Sakaki teach in figure 9 an adhesive layer 41A attached to the stress-balancing layer 2 (para. 0136), which adhesive layer may be marked by a laser (an intended use).

Response to Arguments

Applicant's arguments filed 01/13/2006 have been fully considered but they are not persuasive.

The argument that "Sakaki et al. does not describe, either expressly or inherently, either a stress-balancing layer or a force balancing layer comprising at least one of ... a tape material for balancing stresses in more than one direction" is not persuasive. Sakaki clearly illustrates in FIG. 8 and describes in paragraphs 123-134 the stress or force balancing layer 2 comprising a tape material. Particularly paragraph 132 discloses "a resin film 2 and a spacer tape 36 from a

[1] Any solid material will naturally balance stress in more that one direction. As evidence of this see Mechanics of Materials by E. P. Popov (Exhibit A). Popov on page 35 discloses that "**Poisson's Ratio.** In addition to the deformation of material in the direction of the applied force, ... a certain amount of lateral (transverse) expansion or contraction takes place." Therefore, any balancing of forces in one direction will naturally balance forces and stresses in more than on direction.

reel 35A." As stated above, Popov on page 35 discloses that "**Poisson's Ratio**. In addition to the deformation of material in the direction of the applied force, ... a certain amount of lateral (transverse) expansion or contraction takes place." Therefore, any balancing of forces in one direction will naturally balance forces and stresses in more than on direction. In other words as the balancing layer compensates for the bending or stress of the device in one direction it will also compensate for stress in other directions.

The argument that "the Sakaki et al. reference does not identically describe the elements of the inventions calling for stress-balancing layer covering at least a portion of the back side substantially balancing the stress caused by the passivation layer covering a portion of the integrated circuit, the stress-balancing layer comprising at least one of ... a tape material for balancing stresses in more than one direction" is not persuasive. See above and paragraphs 106 and 107. Particularly Sakaki discloses in paragraph 107:

> By creating the resin film 2 from a thermosetting resin in this way, a contraction force generated by hardening/contraction of the resin film 2 is applied to the back surface 1Y of the semiconductor chip 1. Thus, a warp can be prevented from being generated in the semiconductor chip 1 due to hardening/contraction of the resin 7 covering the circuit formation surface 1X of the semiconductor chip 1.

By creating the resin film 2A on the back side, a warp (stress) can be prevented from being generated (balanced) in the semiconductor chip due to hardening/contraction of the resin 7 (passivation layer). Therefore all the elements of the invention have been disclosed.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL.** See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from an examiner should be directed to Primary Examiner Allan Wilson whose telephone number is (571) 272-1738. Examiner Wilson can normally be reached 7:00-4:00 Monday-Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ken Parker can be reached on (571) 272-2298. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Allan R. Wilson
Primary Examiner
28 February 2006